ABSTRACT OF THE DISCLOSURE

A cache memory device for a digital signal processor (DSP) may include a cache memory for providing an instruction to a DSP core of the DSP in response to a request from the DSP core, and another cache memory for enabling a running flag signal in response to an interrupt signal received from the DSP core. The cache memory that enables the running flag may provide a given number of instructions that are different from the first provided instruction, in response to further requests for instructions from the DSP core. Additionally, the cache memory handling the given number of different instructions may disable the running flag signal and cease providing the different instructions when the given number of instructions reaches a threshold value. The above process may be iteratively repeated until there are no further instruction requests from the DSP core to be processed.